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# Using the 2817 Intelligent $E^2PROM$


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# Using the 2817 Intelligent $E^2PROM$

## Contents

## A NEW AND REVOLUTIONARY TYPE OF MEMORY

The Electrically Erasable PROM ($E^2$ PROM) provides the system designer with an inexpensive, non-volatile, in-circuit alterable memory. The $E^2$PROM is superior in reliability to electro-mechanical, non-volatile storage media such as floppy disks. $E^2$PROMs can operate in environments of dust particles, vibration, and wide temperature ranges. The $E^2$PROM offers additional flexibility over UV EPROMs because of in-circuit alterability.

Unlike the previous 2816 $E^2$PROM, the 2817 $E^2$PROM has on-chip address/data latches, auto erase-before-write, and READY/$\overline{BUSY}$ (RDY/$\overline{BUSY}$) output intelligence. These powerful features, discussed later in more detail, are provided to the user through a high level of on-chip integration.

Applications which include remote firmware updating, user-defined functions, calibration constants, configuration parameters, and data logging are easily implemented with the 2817.

For example, in the field of data communications, 2817 $E^2$PROMs are used to store table lookup data that configure the protocol for a given I/O channel. Because the data is stored in $E^2$PROM, the user can quickly reconfigure the I/O channel to a different protocol via an end system keyboard. The 2817 $E^2$PROMs provide user flexibility as well as user friendly implementation. Transmission errors and service information can also be logged into the $E^2$PROM.

In navigation or radar systems, program code is often changed to store new flight information. Prior to $E^2$PROMs, the EPROM boards containing the code had to be physically removed to be reprogrammed. With the 2817 $E^2$PROM, reprogramming is easily accomplished because of the in-circuit alterability of $E^2$PROMs.

The realm of potential applications is limited only by the user's imagination. The 2817 $E^2$PROM is already used in an extensive spectrum of applications. $E^2$PROMs are used not only to replace other non-volatile storage mediums in current applications but also to make possible new applications.

## DESIGNING IN THE 2817

The 2817 $E^2$PROM is easy to use. Reading is accomplished in the same manner as with the 2716 EPROM: $\overline{CE}$ = $\overline{OE}$ = LOW, and $\overline{WE}$ = High. The read access time of 250ns makes the 2817 compatible with even high performance microprocessors (such as 8086-2) for zero wait state operation.

Writing to the 2817, however, is much easier than writing to either the 2716 EPROM or the 2816 $E^2$PROM. Writing to a 2716 EPROM is accomplished by first erasing the EPROM completely with ultraviolet light. An EPROM is then programmed before being placed into its target system. When writing to a 2816 $E^2$PROM, the chip is first erased in circuit by applying a high voltage exponential rise time programming pulse and placing logical 1's on the data bus. After erasure, the 2816 $E^2$PROM is then programmed with another programming pulse.

By contrast, the 2817 is as simple as writing to a RAM: $\overline{CE}$ = $\overline{WE}$ = LOW, $\overline{OE}$ = HIGH. All the control signals initiating the write cycle are TTL level. Like a RAM, the user does not have to erase the memory location before writing to it; the erase-before-write is performed automatically by on-chip intelligence. The input addresses and data are latched by the $\overline{WE}$ input. Latches make the 2817 $E^2$PROM appear RAM-like to the user even though the programming time for an $E^2$PROM cell is inherently slower than a RAM cell. The on-chip timer generates the internal programming pulse using the external timing capacitor. The RDY/$\overline{BUSY}$ output goes low to indicate that a write operation is in progress. The system CPU can then continue its normal processing work until the 2817's RDY/$\overline{BUSY}$ output goes back high, at which time another byte write or read operation can be initiated.

## SIMPLE INTERFACE REQUIREMENTS

The 2817 does not need the external timing and complex digital switching logic that is required for interfacing the 2816 to a microprocessor bus. From an external circuitry standpoint, all that is needed is a static $V_{PP}$ 21V supply and a write protection circuit. The 2817 requires a static 21V for both read cycles and write operations. It will be possible to read the 2817 with either 5V or 21V on $V_{PP}$) on parts shipped after January 1983. The write protection circuit is needed to prevent data loss during $V_{CC}$ power transitions. The TTL SSI devices that are normally used in systems to drive the $\overline{CE}$ and $\overline{WE}$ inputs are typically unstable when $V_{CC}$ is below 4 volts. These TTL drivers could cause a spurious write operation to occur when $V_{CC}$ is below normal operating level, and a data byte would be lost (see Figure 1). To prevent data loss under such conditions, the $\overline{WE}$ input should be maintained at $V_{IH}$ (or equal to $V_{CC}$) during $V_{CC}$ power transitions (see Figure 2).

## A WRITE PROTECTION CIRCUIT EXAMPLE

A circuit satisfying the condition of $\overline{WE}$ at $V_{IH}$ (or $V_{CC}$) to prevent a spurious write operation is shown in Figure 3. The components used are all readily available, inexpensive, and occupy little board space. This circuit has been tested extensively at 25 °C.

The circuit operates by monitoring system $V_{CC}$ and using it to qualify the system $\overline{WE}$ output signal. The zener diode determines when transistor Q1 turns on and off. When $V_{CC}$ is below 4.5V the zener is not have sufficient voltage across it to remain on. When the zener is not conducting, Q1 is off. Q2 is then turned on, bringing the base of Q3 low. Q3 is turned off which causes the $\overline{WE}$ input of the 2817 to be pulled to $V_{CC}$. In this condition the system $\overline{WE}$ signal will not be able to affect the $\overline{WE}$ input of the 2817. When $V_{CC}$ is above 4.5V, Q1 is on, Q2 is off, and Q3 acts as an inverter, permitting the system $\overline{WE}$ signal to pass through.

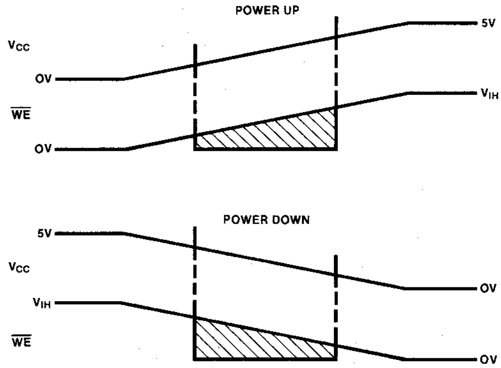



**Figure 1. Typical TTL Driver Instability during $V_{CC}$ Power Transitions**

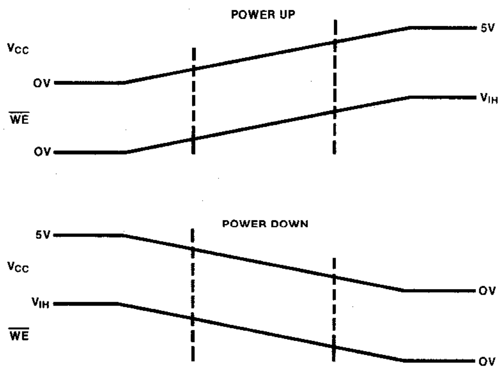



**Figure 2. Controlled $\overline{WE}$ during $V_{CC}$ Power Transitions**

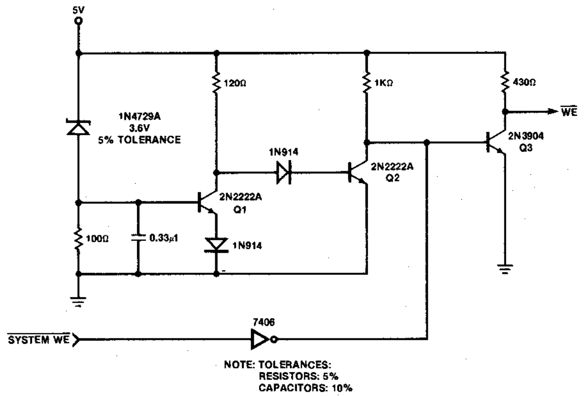



**Figure 3. 2817 Write Protection Circuit**

## ADVANTAGE OF STATIC 21V

With the 2817 the system designer can leave $V_{PP}$ on during normal operation rather than switch $V_{PP}$ on and off. The 2817 on-chip intelligence automatically generates and shapes the programming pulses internally from the external 21V static supply. The 2816 requires external logic to produce a switching $V_{PP}$ signal to accomplish the same task. If the 2817's $V_{PP}$ had to be switched on for write cycles there would be some delay involved in bringing $V_{PP}$ up to 21V. There would also be noise coupled into the surrounding TTL circuitry resulting from the fast switching of a high voltage.

Since it is generally a good practice to decouple any power supply, it is recommended that $V_{PP}$ (Pin 1) be decoupled with a 0.1 microfarad capacitor.

### 21V Is Easy To Obtain

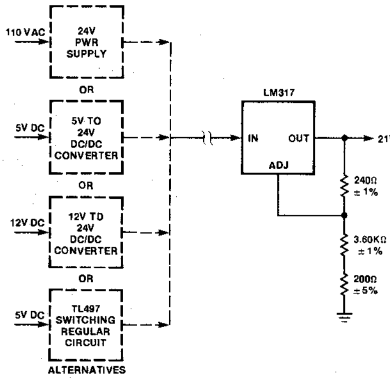
The 21V for $V_{PP}$ can come from a number of sources. A separate AC input 21V supply could be used. A less expensive alternative for a small array of 2817's is a DC to DC converter. Modular 5V to 21V (or 24V) converters are available from various power supply vendors that can provide anywhere from 30mA to 200mA. (See Appendix A) An example would be the ELPAC/TDK CE-0299: It costs from \$6 to \$14, can supply 3 2817's (1 device in write mode = 15mA, 2 devices in read or standby mode = 16mA), and fits into a 24 dip socket. (If a 28 pin socket is used instead of a 24 pin socket, the former could be used as an additional memory socket when the circuit is upgraded to the 5V-only 2817A.)

The TL497A-based circuit shown in the 2817 data sheet costs about \$4 in large quantities. It can provide enough current for 8 devices.

## LARGE ARRAYS

An array of 8 2817's will require only 71mA (15mA for one device in write mode, 56mA for 7 devices in standby or read mode).

The TL497A based circuit discussed above can be used. It will output 21V or 24V. There are also numerous 5V to 24V converters available at this current rating and higher. To provide a regulated 21V output from these converters an LM317 voltage regulator can be used as shown in Figure 4.




Note: All resistors are 1/4 Watt.

**Figure 4. Voltage Regulator For Supplying $V_{PP}$ In Large Arrays**

## CONNECTING THE RDY/BUSY OUTPUT TO THE SYSTEM

The 2817's on-chip intelligence controls the programming cycle and provides a system feedback signal. When the address and data are latched into the 2817 by the WE input pulse, the RDY/$\overline{\text{BUSY}}$ output goes low indicating that a write operation is in progress. After a predetermined amount of time has elapsed to insure successful programming, the RDY/$\overline{\text{BUSY}}$ output returns high to indicate the write operation is complete.

The system CPU can deal with the 2817 RDY/$\overline{\text{BUSY}}$ output in one of two ways: the output can be used as an interrupt to the CPU, or it can be polled.

If the CPU is not needed for system functions while the $E^2$PROM write cycles are in progress, then polled mode would be acceptable since it usually requires less software and/or hardware than interrupt mode. Otherwise, an interrupt-driven mode should be used.

Figures 5, 6, and 7 show how the RDY/$\overline{\text{BUSY}}$ output could be used as an interrupt in 8088, 8085A, or 8051-based systems, respectively. Figures 8 and 9 show hardware diagrams for polled mode operation.

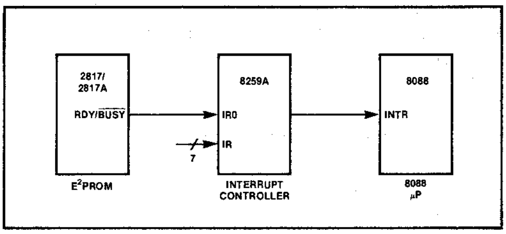



Figure 5. Interrupt-Driven 8088 System

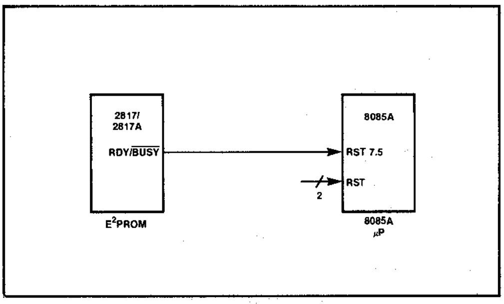



Figure 6. Interrupt-Driven 8085A System

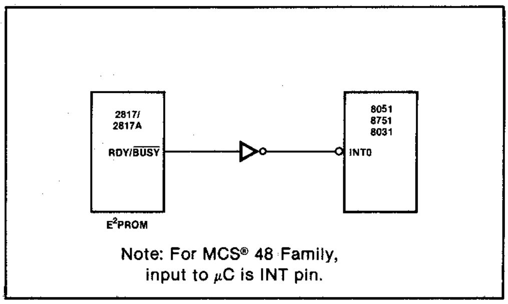



Figure 7. Interrupt-Driven Microcontroller System

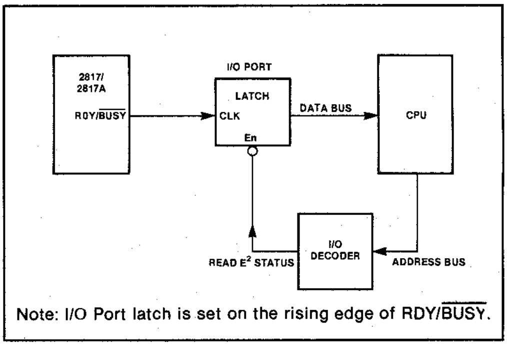



Figure 8. Polled Mode, General

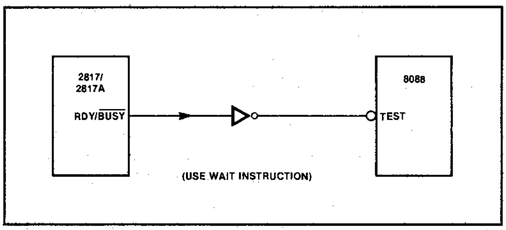



Figure 9. Polled Mode For 8088 System

Polled mode with the 8088 can be done easily and effectively with minimal software and hardware as shown in Figure 9. To write to the 2817, simply do the following:

```
MOV   AL, DATA BYTE   ;LOAD AL REG WITH DATA
MOV   E2PROM, AL      ;WRITE IT TO E2
WAIT                  ;WAIT UNTIL WRITE OPERATION
                      ;IS DONE
```

The 8088 will remain in a wait state while the test input is high (RDY/$\overline{\text{BUSY}}$ is low). When the test input returns low, program execution will continue with the next instruction following 'WAIT'.

The following two steps describe how a data block can be transferred from RAM to $E^2$PROM in an interrupt-driven system. The operation is initiated by two actions: (1) a software pointer is loaded indicating the target $E^2$PROM data block (2) a system memory write cycle is initiated to the first address of the $E^2$PROM data block. Normal processing then continues while an interrupt subroutine such as the one shown in Figure 10 does the rest.

As each $E^2$PROM write operation is completed, the interrupt subroutine is called up via the RDY/$\overline{\text{BUSY}}$ output to write the next byte. When the data block has been completely transferred to $E^2$PROM, a software busy flag is cleared to indicate the status to the CPU.

## FUTURE UPGRADABILITY TO THE 5V-ONLY 2817A

A powerful set of intelligence is currently integrated onto the 2817. In the future, the circuitry to generate the programming voltage from a 5 volt supply will be integrated on-chip with the 2817A. Figure 11 a) and b) shows how to design in a jumper and a resistor location for a 2817 PC board layout so that the 5V-only 2817A can be easily installed in the future. Table I shows the pinout differences between the two devices.

The 2817A has a write protection circuit on-chip so that the external circuit in Figure 3 is not required. This circuit can remain on board and be used with the 2817A if desired.

The RDY/$\overline{\text{BUSY}}$ pin of the 2817A is an open drain output. The design enables the user to tie the RDY/$\overline{\text{BUSY}}$ line from 2 or more 2817A's together. If two 2817A's are tied together, the RDY/$\overline{\text{BUSY}}$ line will not go back high until both 2817A's are successfully programmed. This is ideal in 16 bit bus architectures. The 7.5K resistor shown is a minimum value for 1 TTL load, since the total sink current should not exceed the device rating: 2.1mA @ VOL = 0.4V.

The resistor value can be calculated as follows:

$$R_{(PULLUP)} = \frac{4.6V}{2.1\ MA - IIL}$$

Where IIL = The total VIL input current of all devices connected to RDY/$\overline{\text{BUSY}}$.

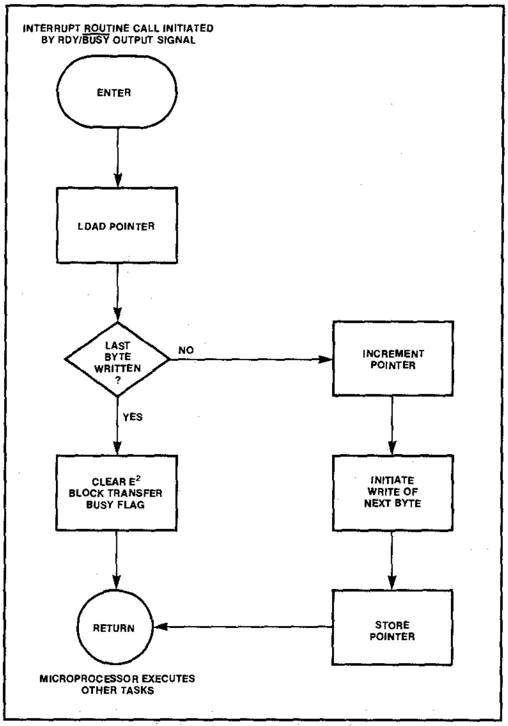



**Figure 10. Interrupt Subroutine Servicing Blocks Transfer To 2817**

**Table 1. Differences in Pinout of 2817 and 2817A**

| | PINS | | |
|---|---|---|---|
| **Device** | **1** | **2** | **26** |
| 2817 | VPP | RDY/$\overline{\text{BUSY}}$ | TIMING CAP |
| 2817A | RDY/$\overline{\text{BUSY}}$ | NC | NC |

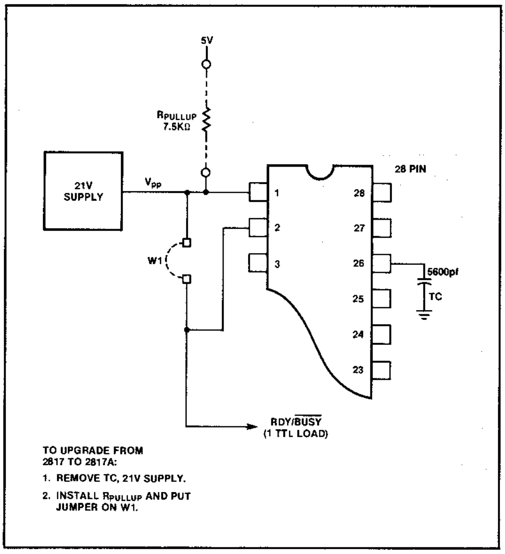



Figure 11A. Upgrade Layout For 2817/2817A

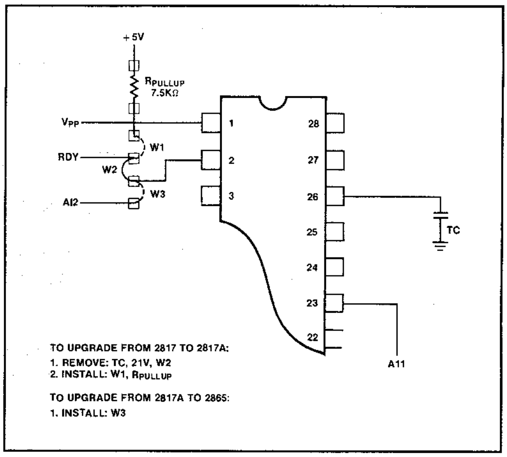



Figure 11B. Upgrade Layout For 2817/2817A/2865

| THIS IS A FEW OF THE MANY 5V TO 21V (OR 24V) CONVERTERS THAT ARE AVAILABLE. | | | | |
|---|---|---|---|---|
| DESCRIPTION | $V_{OUT}$ | $I_{OUT}$ | EST. COST (1) | SIZE |
| ELPAC/TDK CE-0299 | 21V | 35 MA | $ 6 (14) | 24 PIN DIP |
| DATEL UPM-24/40-D5 | 24V | 40 MA | $29 (46) | 2.5 SQ IN |
| RELIABILITY, INC. VA12-12 | 23V | 40 MA | $17 (24) | 24 PIN DIP |
| INTRONICS DCR 5/12-12 | 24V | 80 MA | $36 (40) | 24 PIN DIP |

NOTES: 1. The numbers in the 'cost' column indicated both large and small quantities as follows: Large Qty's (small qty's).

## VENDOR INFORMATION

| VENDOR | ADDRESS | PHONE NUMBER |
|---|---|---|
| ELPAC/TDK POWER SYSTEM | 3131 S. STANDARD AVE.<br>SANTA ANA, CA 92705 | (714) 979-4440 |
| DATEL/INTERSIL | 11 CABOT BLVD.<br>MANSFIELD, MA. 02048 | (617) 339-9341<br>(617) 828-8000 |
| RELIABILITY, INC. OF TEXAS | P.O. BOX 218370<br>HOUSTON, TEXAS 77218 | (713) 492-0550 |
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